REMARKS

Claims 1 and 7 been amended. No claims have been canceled or added. Accordingly, claims 1-12 are currently pending in the above-identified application. Applicants' wish to thank the Examiner for correcting the status of the claims in the previous amendment.

Priority

Applicants appreciate the Examiner's acknowledgment of the claim for priority and safe receipt of the certified priority document.

Claim Objections

The claims have been amended to overcome the Examiners' objections.

35 U.S.C. §103

Claims 1-3 and 7-9 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (EP 1,132,805) in view of Obara (JP 11-296313). Claims 4 and 10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (EP 1,132,805) in view of Obara (JP 11-296313) as applied to claims 2 and 8 and further in view of Fan (U.S. Pub. No.

2002/0054567). Claims 5 and 11 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (EP 1,132,805) in view of Obara (JP 11-296313) as applied to claims 1 and 7 and further in view of Rakvic (U.S. Pub. No. 2002/0188804). Finally, claims 6 and 12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Fujimoto (EP 1,132,805) in view of Obara (JP 11-296313) as applied to claims 2 and 8 and further in view of Fan (U.S. Pub. No. 2002/0054567) and Jantz (U.S. Patent No. 5,937,428). These rejections are traversed as follows.

The present invention is directed to a disk array controller that selects an optimum connection route between a host computer and a cache memory of a disk array controlling unit. Therefore, even if a data copy operation is performed between one cache memory section and another cache memory section via a mutual connection network, data can be transferred from a host computer to the cache memory section without any problems. The independent claims have been amended to recite that the host switch interface section selects a relay destination for data which is sent from the host computer to the cache memory section in accordance with load conditions of a path to the cache memory section in the first disk array controlling unit through the first disk array

controlling unit, through the second disk array controlling unit and through another disk array controlling unit.

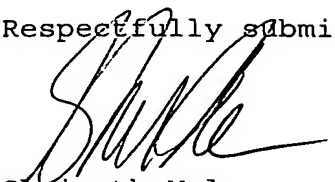
As admitted by the Examiner from page 4, line 17 to page 5, line 5, Fujimoto does not disclose a host switch interface section connected to a host computer and interfacing with the host switch interface sections of the disk array controlling unit as required by claim 1. In order to cure this deficiency, the Examiner relies upon Obara's disclosure. Obara discloses a storage sub-system that attains a load distribution between controllers by rearranging volumes. However, Obara does not disclose or suggest that a host switch interface section selects a path to a cache memory section in accordance with load conditions of the path to the cache memory section on the mutual connection network. As such, it is submitted that the attempted combination of these two references fails to render the presently claimed invention unpatentable.

The attempted application of the additional references to various dependent claims does not overcome the deficiencies noted above with respect to the primary combination of Fujimoto and Obara. As such, it is submitted that the dependent claims also patentably define the present invention over the cited art.

Conclusion

In view of the foregoing amendments and remarks, Applicants contend that the above-identified application is now in condition for allowance. Accordingly, reconsideration and reexamination are respectfully requested.

Respectfully submitted,



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